

11 source supplying a current to the summing node; and
12 an indicator circuit having an input connected to the
13 summing node, wherein the indicator circuit is responsive to
14 changes in the summing node voltage level and generates at an
15 output a logical signal at one state when the summing node
16 voltage level is greater than the predetermined threshold voltage
17 level and generates the logical signal at the output at another
18 state when the summing node voltage level is less than the
19 predetermined threshold voltage level.

Please add the following new claims:

1 --31. A direct current sum bandgap voltage comparator
2 comprising:
3 a summing node;
4 first and second current sources connected between the
5 summing node and a lower power supply; and
6 third and fourth current sources connected between the
7 summing node and an upper power supply,
8 wherein a voltage at the summing node equals a voltage of
9 the upper power supply when a current from the first and second
10 current sources to the summing node exceeds a current from the
11 third and fourth current sources to the summing node, and
12 wherein the voltage at the summing node equals a voltage of
13 the lower power supply when the current from the third and fourth
14 current sources to the summing node exceeds the current from the
15 first and second current sources to the summing node.

1 32. The direct current sum bandgap voltage comparator of claim
2 31, wherein the first current source further comprises:
3 a first field effect transistor connected between the lower
4 power supply and the summing node;
5 a second field effect transistor connected at a source to
6 the lower power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;
9 a third field effect transistor connected at a source to the

lower power supply and connected at a gate to the gate of the first field effect transistor;

a fourth field effect transistors connected at a drain to the drain of the second field effect transistor;

a fifth field effect transistor connected at a drain to a drain of the third field effect transistor and to a gate of the fifth field effect transistor and connected at the gate to a gate of the fourth field effect transistor;

a first bipolar junction transistor connected at a base and a collector to the upper power supply;

a second bipolar junction transistor connected at a base and a collector to the upper power supply and connected at an emitter to a source of the fifth field effect transistor; and

a resistor connected to an emitter of the first bipolar junction transistor and to a source of the fourth field effect transistor.

33. The direct current sum bandgap voltage comparator of claim 32, wherein the first, second, and third field effect transistors are n-channel MOSFETs and the fourth and fifth field effect transistors are p-channel MOSFETs.

34. The direct current sum bandgap voltage comparator of claim 32, wherein the first field effect transistor is sized to generate a current of N times a current flowing through the second field effect transistor.

35. The direct current sum bandgap voltage comparator of claim 31, wherein the first current source further comprises:

a current mirror including a field effect transistor connected between the lower power supply and the summing node, wherein the field effect transistor is sized to generate a current of N times a current flowing through a portion of the current mirror.

36. The direct current sum bandgap voltage comparator of claim 31, wherein the second current source further comprises:

3 a first field effect transistor connected between the lower
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the lower power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;

9 a third field effect transistor connected at a source to the
10 lower power supply and connected at a gate to the gate of the
11 first field effect transistor;

12 a fourth field effect transistor connected at a drain to the
13 drain of the second field effect transistor;

14 a fifth field effect transistor connected at a drain to a
15 drain of the third field effect transistor and to a gate of the
16 fifth field effect transistor and connected at the gate to a gate
17 of the fourth field effect transistor;

18 a bipolar junction transistor connected at a base and a
19 collector to the upper power supply and at an emitter to the
20 source of the fifth field effect transistor; and

21 a resistor connected between a source of the fourth field
22 effect transistor and the upper power supply.

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1 37. The direct current sum bandgap voltage comparator of claim
2 36, wherein the first, second, and third field effect transistors
3 are n-channel MOSFETs and the fourth and fifth field effect
4 transistors are p-channel MOSFETs.

1 38. The direct current sum bandgap voltage comparator of claim
2 31, wherein the third current source further comprises:

3 a first field effect transistor connected between the upper
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the upper power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor;

9 a third field effect transistor connected at a source to the
10 lower power supply and connected at a drain to the drain of the
11 second field effect transistor;

12 a fourth field effect transistor connected at a source to
13 the lower power supply, at a gate to a gate of the third field
14 effect transistor, and at a drain to the gate of the fourth field
15 effect transistor;

16 a fifth field effect transistor connected at a source to the
17 lower power supply;

18 a sixth field effect transistor connected at a drain to the
19 drain of the fourth field effect transistor;

20 a seventh field effect transistor connected at a drain to
21 a drain of the fifth field effect transistor and to a gate of the
22 seventh field effect transistor and connected at the gate to a
23 gate of the sixth field effect transistor;

24 an eighth field effect transistor connected at a drain and
25 at a gate to a source of the seventh field effect transistor and
26 at a source to the upper power supply; and

27 a resistor connected between a source of the sixth field
28 effect transistor and the upper power supply.

1 39. The direct current sum bandgap voltage comparator of claim
2 38, wherein the first, second, sixth, seventh, and eighth field
3 effect transistors are p-channel MOSFETs and the third, fourth
4 and fifth field effect transistors are n-channel MOSFETs.

1 40. The direct current sum bandgap voltage comparator of claim
2 31, wherein the fourth current source further comprises:

3 a first field effect transistor connected between the upper
4 power supply and the summing node;

5 a second field effect transistor connected at a source to
6 the upper power supply and connected at a gate to a gate of the
7 first field effect transistor and a drain of the second field
8 effect transistor; and

9 a resistor connected between a drain of the second field
10 effect transistor and the lower power supply.

1 41. The direct current sum bandgap voltage comparator of claim
2 40, wherein the first and second field effect transistors are p-
3 channel MOSFETs.